

LP8345

Low Dropout, Low IQ, 500mA CMOS Linear Regulator

General Description

The LP8345 low-dropout CMOS linear regulator are available in 5V, 3.3V, 2.5V, 1.8V or adjustable output versions. Packaged in our 6ld LLP package and 3ld DPAK they can deliver up to 500mA output current.

Typical dropout voltage @ 500mA is 210mV for the 5.0V version, 270mV for the 3.3V version and 335mV for the 2.5V version.

The devices include a zener trimmed bandgap voltage reference, foldback current limiting and thermal overload limiting.

The LP8345 features a PMOS output transistor which unlike PNP type low dropout regulators requires no base drive current. This allows the device ground current to remain less than 50µA over operating temperature, supply voltage and irrespective of the load current.

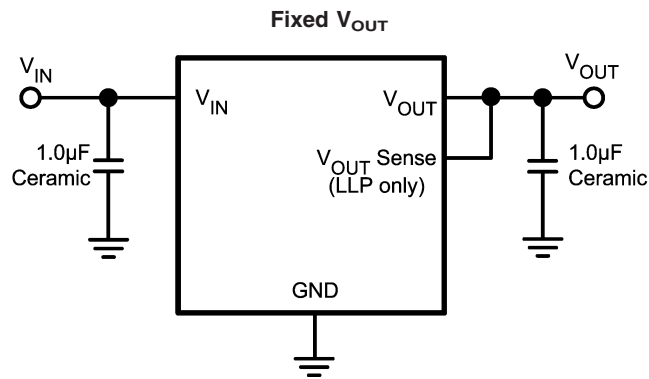
Features

- ±1.5% Typical V_{OUT} tolerance
- 210mV Typical Dropout @ 500mA ($V_O = 5V$)
- Wide Operating Range 2.7V to 10V
- Internal 500mA PMOS Output Transistor
- 19µA Typical Quiescent Current
- Thermal Overload Limiting
- Foldback Current Limiting
- Zener Trimmed Bandgap Reference
- Space saving LLP package
- Temperature Range
 - LP8345C 0°C to 125°C
 - LP8345I -40°C to 125°C

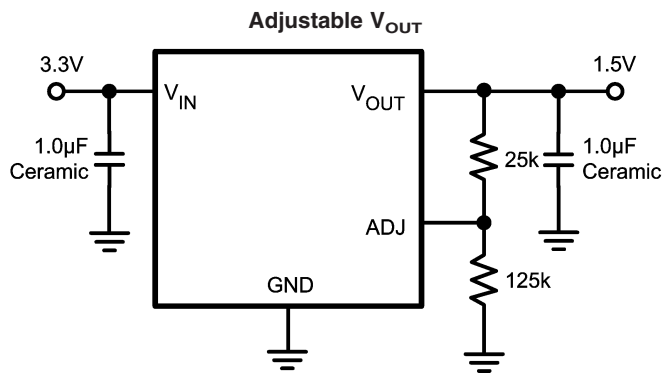
Applications

- Hard Disk Drives
- Notebook Computers
- Battery Powered Electronics
- Portable Instrumentation

Typical Applications



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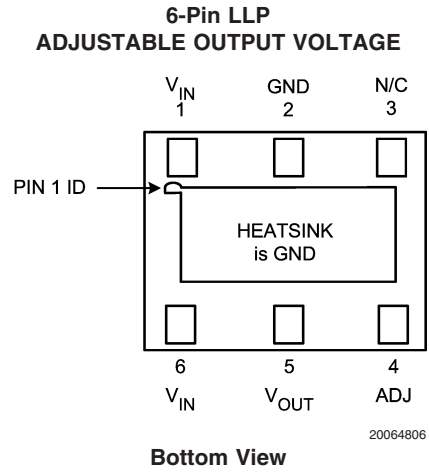
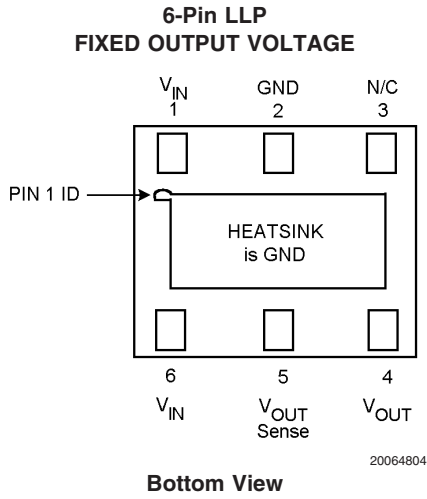


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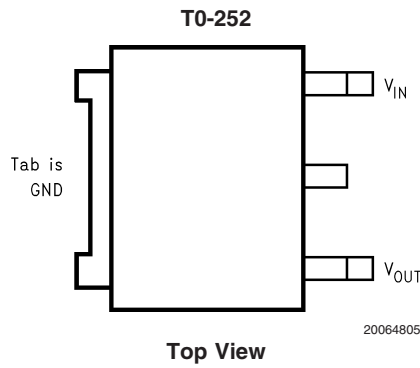
Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
6-Pin LLP	LP8345CLD-ADJ	L045B	1k Units Tape and Reel	LDE06A
	LP8345CLDX-ADJ		4.5k Units Tape and Reel	
	LP8345CLD-1.8	L046B	1k Units Tape and Reel	
	LP8345CLDX-1.8		4.5k Units Tape and Reel	
	LP8345CLD-2.5	L047B	1k Units Tape and Reel	
	LP8345CLDX-2.5		4.5k Units Tape and Reel	
	LP8345CLD-3.3	L048B	1k Units Tape and Reel	
	LP8345CLDX-3.3		4.5k Units Tape and Reel	
	LP8345CLD-5.0	L049B	1k Units Tape and Reel	
	LP8345CLDX-5.0		4.5k Units Tape and Reel	
	LP8345ILD-ADJ	L073B	1k Units Tape and Reel	
	LP8345ILD-ADJ		4.5k Units Tape and Reel	
	LP8345ILD-1.8	L074B	1k Units Tape and Reel	
	LP8345ILD-1.8		4.5k Units Tape and Reel	
	LP8345ILD-2.5	L075B	1k Units Tape and Reel	
	LP8345ILD-2.5		4.5k Units Tape and Reel	
	LP8345ILD-3.3	L076B	1k Units Tape and Reel	
	LP8345ILD-3.3		4.5k Units Tape and Reel	
	LP8345ILD-5.0	L077B	1k Units Tape and Reel	
	LP8345ILD-5.0		4.5k Units Tape and Reel	
3-Pin DPAK	LP8345CDT-1.8	LP8345CDT-1.8	75 Units/Rail	TD03B
	LP8345CDTX-1.8		2.5k Units Tape and Reel	
	LP8345CDT-2.5	LP8345CDT-2.5	75 Units/Rail	
	LP8345CDTX-2.5		2.5k Units Tape and Reel	
	LP8345CDT-3.3	LP8345CDT-3.3	75 Units/Rail	
	LP8345CDTX-3.3		2.5k Units Tape and Reel	
	LP8345CDT-5.0	LP8345CDT-5.0	75 Units/Rail	
	LP8345CDTX-5.0		2.5k Units Tape and Reel	
	LP8345IDT-1.8	LP8345IDT-1.8	75 Units/Rail	
	LP8345IDTX-1.8		2.5k Units Tape and Reel	
	LP8345IDT-2.5	LP8345IDT-2.5	75 Units/Rail	
	LP8345IDTX-2.5		2.5k Units Tape and Reel	
	LP8345IDT-3.3	LP8345IDTX-3.3	75 Units/Rail	
	LP8345IDT-3.3		2.5k Units Tape and Reel	
	LP8345IDTX-5.0	LP8345IDTX-5.0	75 Units/Rail	
	LP8345IDT-5.0		2.5k Units Tape and Reel	

Connection Diagrams



Note: V_{IN} Pins (Pin 1 & 6) must be connected together externally for full 500mA operation (250mA max per pin).
 V_{OUT} Sense (Pin 5) must be connected to V_{OUT} (Pin 4).



Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{IN} , V_{OUT} , V_{OUT} Sense, ADJ	-0.3V to 12V
Storage Temperature Range	-65°C to 160°C
Junction Temperature (T_J)	150°C
Power Dissipation	(Note 3)
ESD Rating	

Human Body Model (Note 6)	2kV
Machine Model	200V

Operating Ratings(Notes 1, 2)

Supply Voltage	2.7 to 10V
Temperature Range	
LP8345C	0°C to 125°C
LP8345I	-40°C to 125°C

LP8345C Electrical Characteristics

Unless otherwise specified all limits guaranteed for $V_{IN} = V_O + 1V$, $C_{IN} = C_{OUT} = 10\mu F$, $T_J = 25^\circ C$. **Boldface** limits apply over the full operating temperature range of $T_J = 0^\circ C$ to 125°C

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
V_{IN}	Input Voltage	LP8345-ADJ, 1.8, 2.5 LP8345-3.3, 5.0	2.7		10 10	V
V_{OUT}	Output Voltage	LP8345-ADJ, ADJ = OUT $I_{OUT} = 10mA$, $V_{IN} = 2.7V$, $T_J = 25^\circ C$ $100\mu A \leq I_{OUT} \leq 500mA$, $2.7V \leq V_{IN} \leq V_{OUT} + 4V$	1.231 1.213	1.250	1.269 1.288	V
		LP8345-1.8 $I_{OUT} = 10mA$, $V_{IN} = 2.8V$, $T_J = 25^\circ C$ $100\mu A \leq I_{OUT} \leq 500mA$, $2.8V \leq V_{IN} \leq 6V$	1.773 1.746	1.800	1.827 1.854	V
		LP8345-2.5 $I_{OUT} = 10mA$, $V_{IN} = 3.5V$, $T_J = 25^\circ C$ $100\mu A \leq I_{OUT} \leq 500mA$, $3.5V \leq V_{IN} \leq 6.5V$	2.463 2.425	2.500	2.538 2.575	V
		LP8345-3.3 $I_{OUT} = 10mA$, $V_{IN} = 4.3V$, $T_J = 25^\circ C$ $100\mu A \leq I_{OUT} \leq 500mA$, $4.3V \leq V_{IN} \leq 7.5V$	3.250 3.201	3.300	3.350 3.399	V
		LP8345-5.0 $I_{OUT} = 10mA$, $V_{IN} = 6V$, $T_J = 25^\circ C$ $100\mu A \leq I_{OUT} \leq 500mA$, $6V \leq V_{IN} \leq 9V$	4.925 4.850	5.000	5.075 5.150	V
ΔV_O	Load Regulation	LP8345-ADJ, ADJ=OUT $I_{OUT} = 1mA$ to 500mA, $V_{IN} = 2.7V$		6	20	mV
		LP8345-1.8 $I_{OUT} = 1mA$ to 500mA, $V_{IN} = 2.8V$		7	20	
		LP8345-2.5 $I_{OUT} = 1mA$ to 500mA, $V_{IN} = 3.5V$		9	30	
		LP8345-3.3 $I_{OUT} = 1mA$ to 500mA, $V_{IN} = 4.3V$		12	35	
		LP8345-5.0 $I_{OUT} = 1mA$ to 500mA, $V_{IN} = 6V$		14	40	
ΔV_O	Line Regulation	$V_{OUT} + 0.5V \leq V_{IN} \leq 10V$, $I_{OUT} = 25mA$ (Note 7)		4	15	mV
$V_{IN} - V_O$	Dropout Voltage (Note 7) (Note 8)	LP8345-2.5 $I_{OUT} = 500mA$		335	650	mV
		LP8345-3.3 LP8345-ADJ, $V_{OUT} = 3.3V$, $I_{OUT} = 500mA$		270	500	
		LP8345-5.0 $I_{OUT} = 500mA$		210	400	
I_Q	Quiescent Current	$V_{IN} \leq 10V$		19	50	μA
	Minimum Load Current	$V_{IN} - V_{OUT} \leq 4V$			100	μA
I_{LIMIT}	Foldback Current Limit	$V_{IN} - V_{OUT} > 5V$		450		mA
		$V_{IN} - V_{OUT} < 4V$		1200		

LP8345C Electrical Characteristics (Continued)

Unless otherwise specified all limits guaranteed for $V_{IN} = V_{O+} + 1V$, $C_{IN} = C_{OUT} = 10\mu F$, $T_J = 25^\circ C$. **Boldface** limits apply over the full operating temperature range of $T_J = 0^\circ C$ to $125^\circ C$

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
	Ripple Rejection Ratio	$V_{IN} (dc) = V_{OUT} + 2V$ $V_{IN} (ac) = 1V_{P-P} @ 120Hz$	48	55		dB
T_{SD}	Thermal Shutdown Temp. Thermal Shutdown Hyst.			160 10		$^\circ C$
	ADJ Input Leakage Current	$V_{ADJ} = 1.5V$ or $0V$		± 0.01	± 100	nA
	V_{OUT} Leakage Current	LP8345-ADJ ADJ = OUT, $V_{OUT} = 2V$, $V_{IN} = 10V$			10	μA
		LP8345-1.8, $V_{OUT} = 2.5V$, $V_{IN} = 10V$			10	
		LP8345-2.5, $V_{OUT} = 3.5V$, $V_{IN} = 10V$			10	
		LP8345-3.3, $V_{OUT} = 4V$, $V_{IN} = 10V$			10	
		LP8345-5.0, $V_{OUT} = 6V$, $V_{IN} = 10V$			10	
e_n	Output Noise	10Hz to 10kHz, $R_L = 1k\Omega$, $C_{OUT} = 10\mu F$		250		μV_{rms}

LP8345I Electrical Characteristics

Unless otherwise specified all limits guaranteed for $V_{IN} = V_{O+} + 1V$, $C_{IN} = C_{OUT} = 10\mu F$, $T_J = 25^\circ C$. **Boldface** limits apply over the full operating temperature range of $T_J = -40^\circ C$ to $125^\circ C$

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
V_{IN}	Input Voltage	LP8345-ADJ, 1.8, 2.5 LP8345-3.3, 5.0	2.7		10 10	V
V_{OUT}	Output Voltage	LP8345-ADJ, ADJ = OUT $I_{OUT} = 10mA$, $V_{IN} = 2.7V$, $T_J = 25^\circ C$ $100\mu A \leq I_{OUT} \leq 500mA$, $2.7V \leq V_{IN} \leq V_{OUT} + 4V$	1.231 1.213	1.250	1.269 1.288	V
		LP8345-1.8 $I_{OUT} = 10mA$, $V_{IN} = 2.8V$, $T_J = 25^\circ C$ $100\mu A \leq I_{OUT} \leq 500mA$, $2.8V \leq V_{IN} \leq 6V$	1.773 1.746	1.800	1.827 1.854	V
		LP8345-2.5 $I_{OUT} = 10mA$, $V_{IN} = 3.5V$, $T_J = 25^\circ C$ $100\mu A \leq I_{OUT} \leq 500mA$, $3.5V \leq V_{IN} \leq 6.5V$	2.463 2.425	2.500	2.538 2.575	V
		LP8345-3.3 $I_{OUT} = 10mA$, $V_{IN} = 4.3V$, $T_J = 25^\circ C$ $100\mu A \leq I_{OUT} \leq 500mA$, $4.3V \leq V_{IN} \leq 7.5V$	3.250 3.201	3.300	3.350 3.399	V
		LP8345-5.0 $I_{OUT} = 10mA$, $V_{IN} = 6V$, $T_J = 25^\circ C$ $100\mu A \leq I_{OUT} \leq 500mA$, $6V \leq V_{IN} \leq 9V$	4.925 4.850	5.000	5.075 5.150	V
		ΔV_O	Load Regulation	LP8345-ADJ, ADJ=OUT $I_{OUT} = 1mA$ to $500mA$, $V_{IN} = 2.7V$		6
LP8345-1.8 $I_{OUT} = 1mA$ to $500mA$, $V_{IN} = 2.8V$				7	20	
LP8345-2.5 $I_{OUT} = 1mA$ to $500mA$, $V_{IN} = 3.5V$				9	30	
LP8345-3.3 $I_{OUT} = 1mA$ to $500mA$, $V_{IN} = 4.3V$				12	35	
LP8345-5.0 $I_{OUT} = 1mA$ to $500mA$, $V_{IN} = 6V$				14	40	
ΔV_O	Line Regulation	$V_{OUT} + 0.5V \leq V_{IN} \leq 10V$, $I_{OUT} = 25mA$ (Note 7)		4	15	mV

LP8345I Electrical Characteristics (Continued)

Unless otherwise specified all limits guaranteed for $V_{IN} = V_O + 1V$, $C_{IN} = C_{OUT} = 10\mu F$, $T_J = 25^\circ C$. **Boldface** limits apply over the full operating temperature range of $T_J = -40^\circ C$ to $125^\circ C$

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
$V_{IN} - V_O$	Dropout Voltage (Note 7) (Note 8)	LP8345-2.5 $I_{OUT} = 500mA$		335	650	mV
		LP8345-3.3 LP8345-ADJ, $V_{OUT} = 3.3V$, $I_{OUT} = 500mA$		270	500	
		LP8345-5.0 $I_{OUT} = 500mA$		210	400	
I_Q	Quiescent Current	$V_{IN} \leq 10V$		19	50	μA
	Minimum Load Current	$V_{IN} - V_{OUT} \leq 4V$			100	μA
I_{LIMIT}	Foldback Current Limit	$V_{IN} - V_{OUT} > 5V$		450		mA
		$V_{IN} - V_{OUT} < 4V$		1200		
	Ripple Rejection Ratio	$V_{IN} (dc) = V_{OUT} + 2V$ $V_{IN} (ac) = 1V_{P-P} @ 120Hz$	48	55		dB
T_{SD}	Thermal Shutdown Temp.			160		$^\circ C$
	Thermal Shutdown Hyst.			10		
	ADJ Input Leakage Current	$V_{ADJ} = 1.5V$ or $0V$		± 0.01	± 100	nA
	V_{OUT} Leakage Current	LP8345-ADJ ADJ = OUT, $V_{OUT} = 2V$, $V_{IN} = 10V$			10	μA
		LP8345-1.8, $V_{OUT} = 2.5V$, $V_{IN} = 10V$			10	
		LP8345-2.5, $V_{OUT} = 3.5V$, $V_{IN} = 10V$			10	
		LP8345-3.3, $V_{OUT} = 4V$, $V_{IN} = 10V$			10	
		LP8345-5.0, $V_{OUT} = 6V$, $V_{IN} = 10V$			10	
e_n	Output Noise	10Hz to 10kHz, $R_L = 1k\Omega$, $C_{OUT} = 10\mu F$		250		μV_{rms}

Note 1: Absolute Maximum ratings indicate limits beyond which damage may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.

Note 2: All voltages are with respect to the potential at the ground pin.

Note 3: Maximum Power dissipation for the device is calculated using the following equations:

$$P_D = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. The value of the θ_{JA} for the LLP package is specifically dependant on the PCB trace area, trace material, and the number of layers and thermal vias. For improved thermal resistance and power dissipation for the LLP package, refer to Application Note AN-1187.

Note 4: Typical Values represent the most likely parametric norm.

Note 5: All limits are guaranteed by testing or statistical analysis.

Note 6: Human body model 1.5k Ω in series with 100pF.

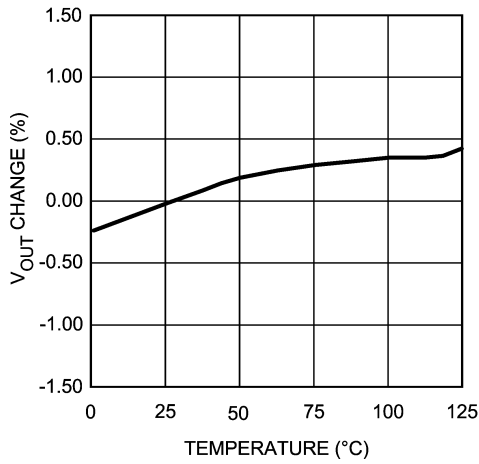
Note 7: Condition does not apply to input voltages below 2.7V since this is the minimum input operating voltage.

Note 8: Dropout voltage is measured by reducing V_{IN} until V_O drops 100mV from its normal value.

Typical Performance Characteristics

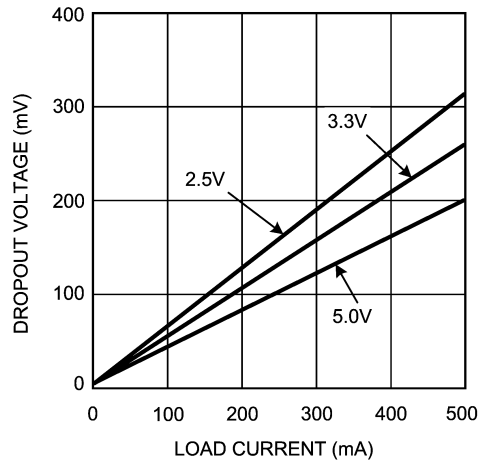
Unless otherwise specified, $V_{IN} = V_O + 1.5V$, $C_{IN} = C_{OUT} = 10\mu F$ X7R ceramic, $T_J = 25^\circ C$

Output Voltage Change vs. Temperature



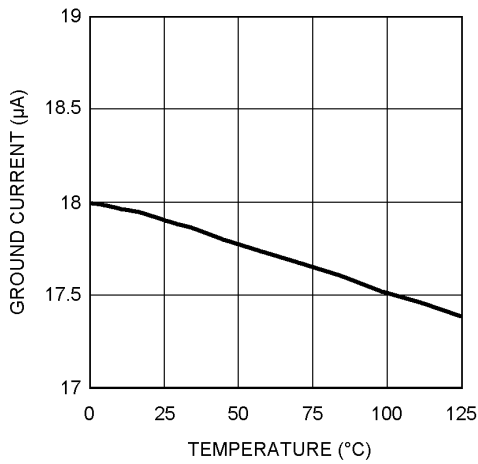
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Dropout Voltage vs. Load Current



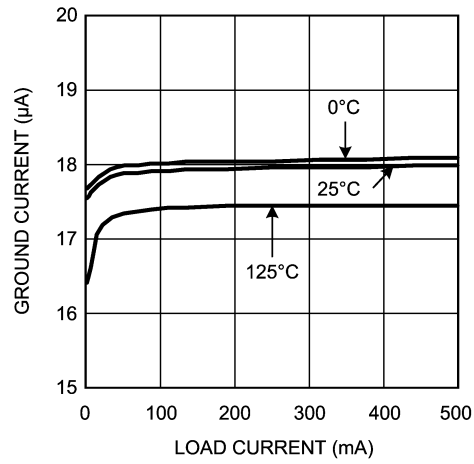
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Ground Current vs. Temperature (I_{LOAD} = 500mA)



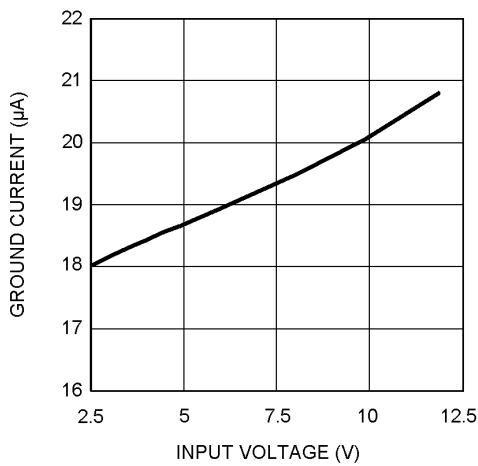
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Ground Current vs. Load Current



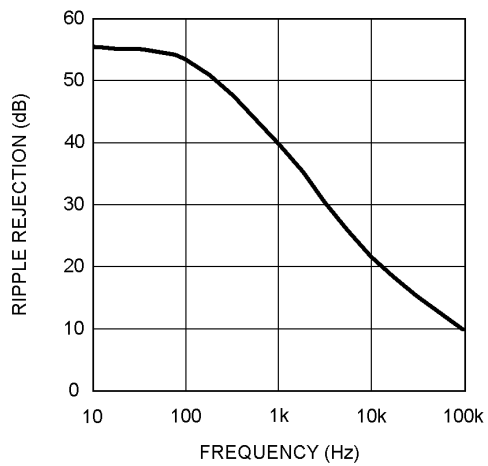
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Ground Current vs. Input Voltage



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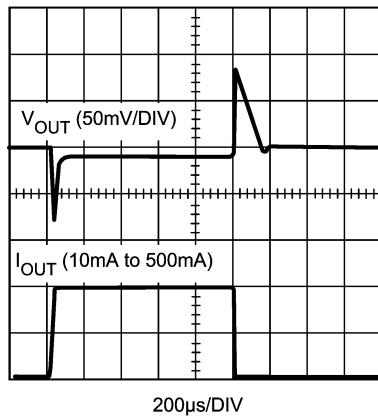
Ripple Rejection Ratio vs. Frequency



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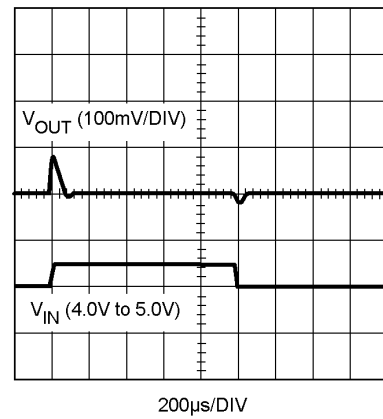
Typical Performance Characteristics (Continued)

Load Transient Response



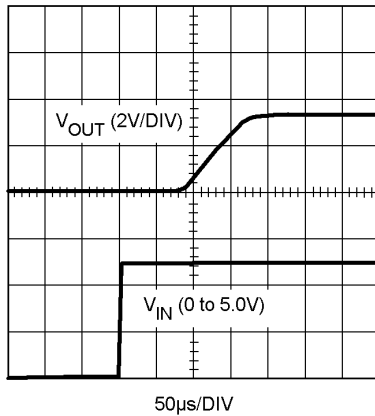
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Line Transient Response



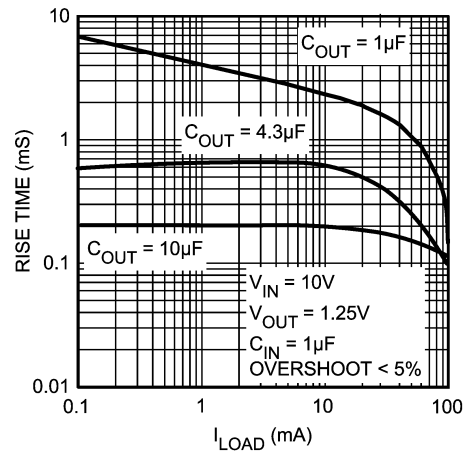
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Start-up Response



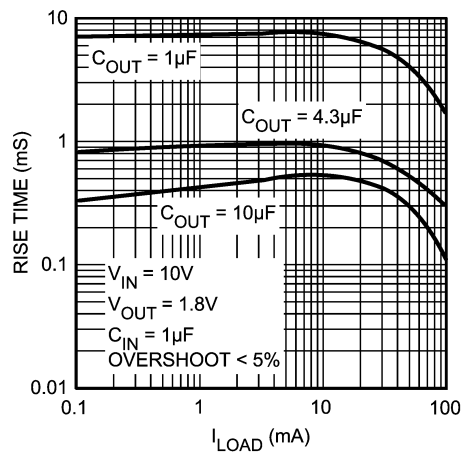
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Minimum Input Voltage Rise Time



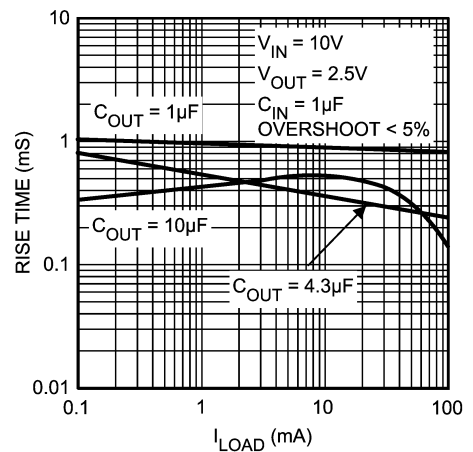
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Minimum Input Voltage Rise Time



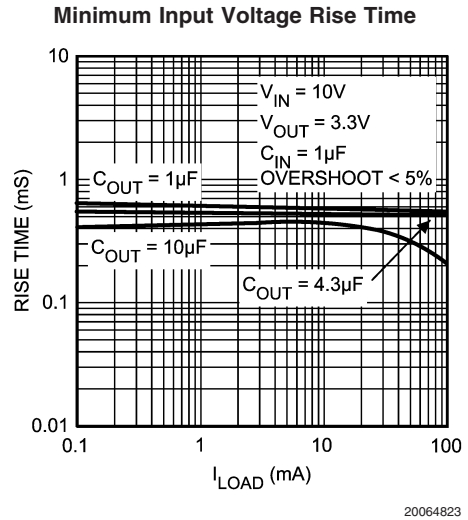
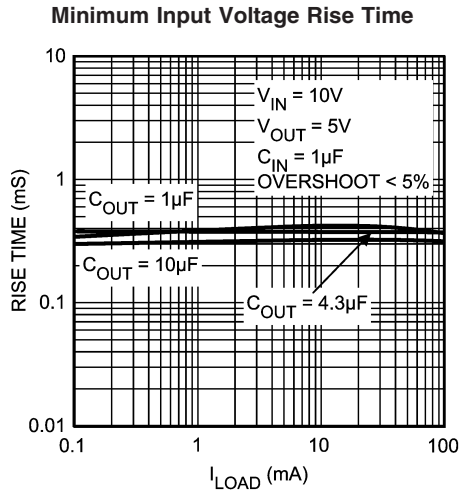
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Minimum Input Voltage Rise Time



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Typical Performance Characteristics (Continued)



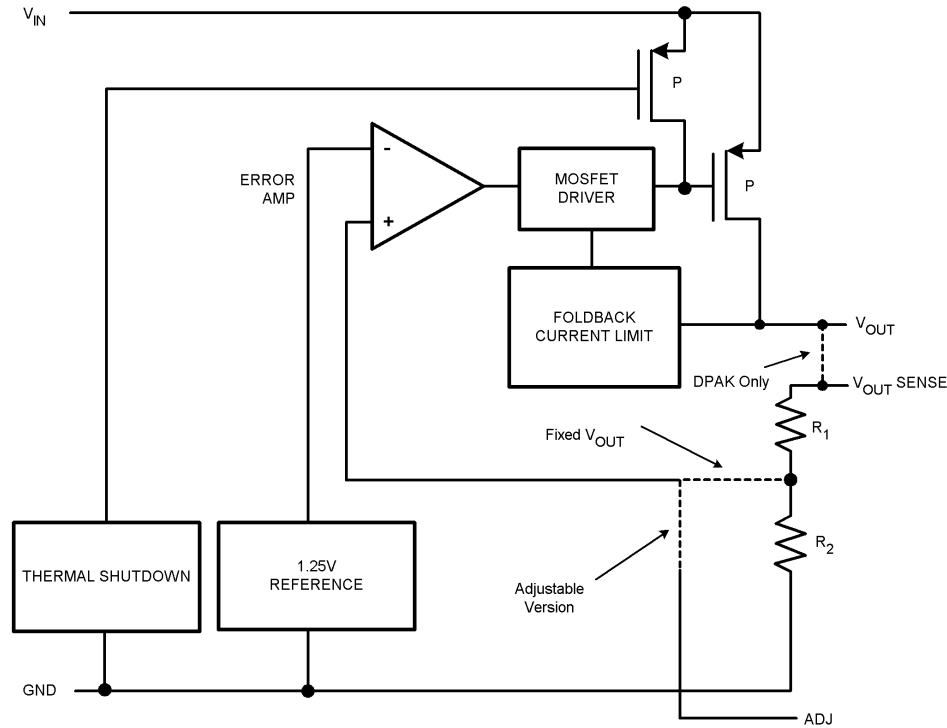
Applications Section

GENERAL INFORMATION

The LP8345 is a low-dropout, low quiescent current linear regulator. As shown in *Figure 1* it consists of a 1.25V reference, error amplifier, MOSFET driver, PMOS pass transistor and for the fixed output versions, an internal feedback network (R_1/R_2). In addition, the device is protected from overload by a thermal shutdown circuit and a foldback current limit circuit.

The 1.25V reference is connected to the inverting input of the error amplifier. Regulation of the output voltage is

achieved by means of negative feedback to the non-inverting input of the error amplifier. Feedback resistors R_1 and R_2 are either internal or external to the device, depending on whether it is a fixed voltage version or the adjustable version. The negative feedback and high open loop gain of the error amplifier cause the two inputs of the error amp to be virtually equal in voltage. If the output voltage changes due to load changes, the error amplifier and MOSFET driver provide the appropriate drive to the pass transistor to maintain the error amplifier's inputs as virtually equal.



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FIGURE 1. LP8345 Functional Block Diagram

EXTERNAL CAPACITOR

An Input capacitor of $1\mu\text{F}$ or greater is required between the LP8345 V_{IN} pin and ground. While $1\mu\text{F}$ will provide adequate bypassing of the V_{IN} supply larger values of input capacitor (i.e. $10\mu\text{F}$) can provide improved bypassing of power supply noise.

Stable operation can be achieved with an output capacitor of $1\mu\text{F}$ or greater, either ceramic X7R dielectric or aluminum/tantalum electrolytic. While the minimum capacitor value is $1\mu\text{F}$, the typical output capacitor values selected range from $1\mu\text{F}$ to $10\mu\text{F}$. The larger values provide improved load-transient response, power supply rejection and stability.

OUTPUT VOLTAGE SETTING (ADJ VERSION ONLY)

The output voltage is set according to the amount of negative feedback (Note that the pass transistor inverts the feedback signal). This feedback is determined by R_1 and R_2 with the resulting output voltage represented by the following equation:

$$V_O = V_{\text{REF}} \left[\frac{R_1}{R_2} + 1 \right]$$

Use the following equation to determine the values of R_1 and R_2 for a desired V_{OUT} ($R_2 = 100\text{k}\Omega$ is recommended).

$$R_1 = R_2 \left[\frac{V_O}{1.25\text{V}} - 1 \right]$$

MINIMUM LOAD CURRENT

A minimum load of $100\mu\text{A}$ is required for regulation and stability over the entire operating temperature range. If actual load current fall below $100\mu\text{A}$ it is recommended that a resistor of value $R_L = V_O/100\mu\text{A}$ be placed between V_O and ground.

Applications Section (Continued)

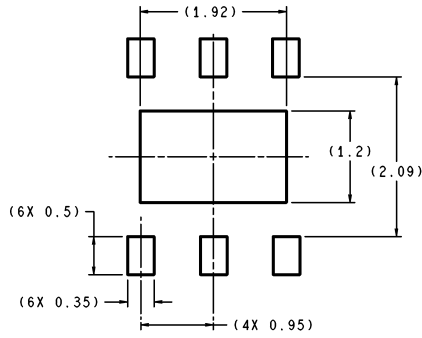
START UP CONSIDERATIONS

Under certain operating conditions, overshoot of V_{OUT} at start-up can occur. The observed overshoot is a function of rise time of V_{IN} waveform, C_{OUT} , start-up load current, and

$V_{IN}-V_{OUT}$ differential. The relationship between these conditions is shown in the Typical Performance Characteristics curves (Minimum Input Voltage Rise Time). V_{IN} rise times above the curve result in <5% overshoot.

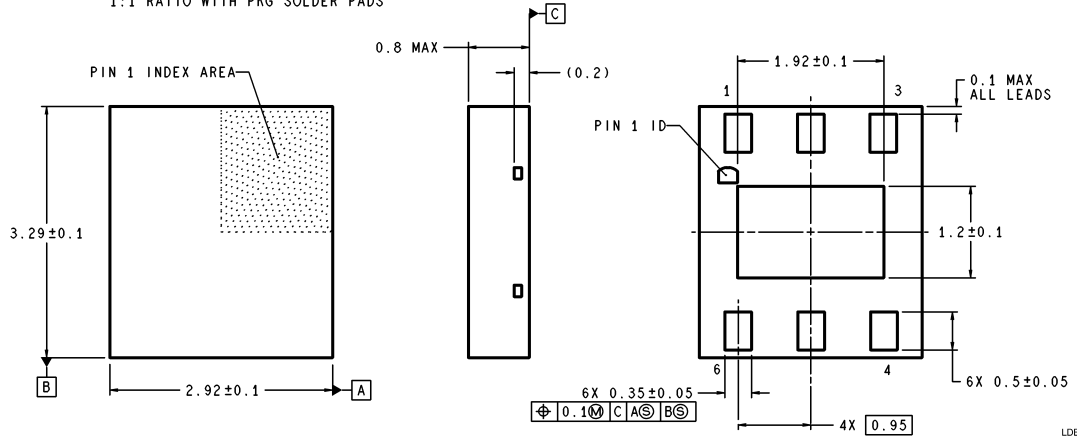
Customers are encouraged to check the suitability of LP8345 in their specific application.

Physical Dimensions inches (millimeters) unless otherwise noted



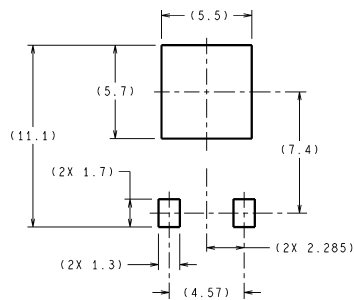
DIMENSIONS ARE IN MILLIMETERS

RECOMMENDED LAND PATTERN
1:1 RATIO WITH PKG SOLDER PADS



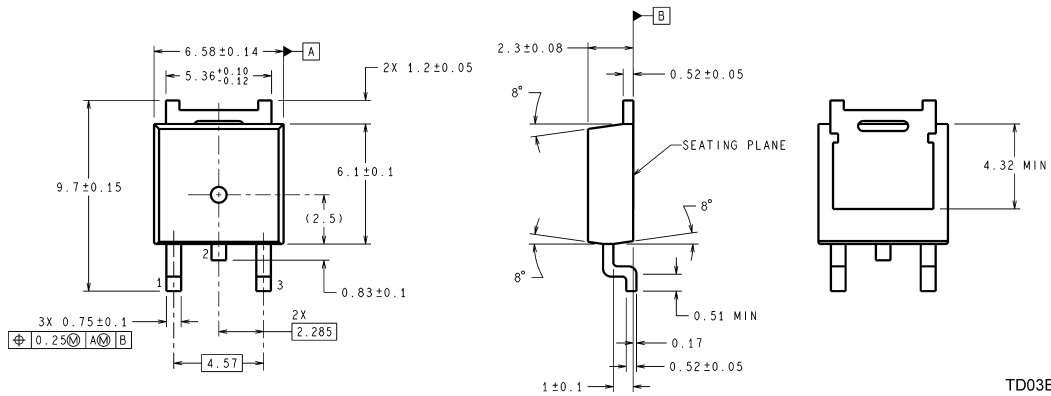
LDE06A (Rev A)

6-Pin LLP
NS Package Number LDE06A



DIMENSIONS ARE IN MILLIMETERS

LAND PATTERN RECOMMENDATION



TD03B (Rev C)

3-Pin DPAK
NS Package Number TD03B

Notes

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.

For the most current product information visit us at www.national.com.

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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